IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kedar PATEL et al.

Title: HIGH DENSITY 3D RAIL STACK ARRAYS AND METHOD OF MAKING

Appl. No.: Unassigned

Filing Date: 2/18/2004

Examiner: Unassigned

Art Unit: Unassigned

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Mail Stop PATENT APPLICATION
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

The USPTO has waived the requirement under 37 CFR 1.98(a)(2)(i) to submit copies of U.S. patents and U.S. patent application publications when citing and submitting an Information Disclosure Statements in a patent application filed after June 30, 2003 and in an international application that has entered the national stage under 37 USC §371 after June 30, 2003. Accordingly, copies of these types of documents are not being supplied in connection with this application. Reference is being made to Pre-OG Notice from Office of Patent Legal Administration dated July 25, 2003, *Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003.*

Applicants submit herewith on Form PTO/SB/08 a listing of the documents cited by or submitted to the U.S. PTO in parent application Serial No. 10/180,046, filed 6/27/2002. As provided in 37 CFR §1.98(d), copies of the documents are not being provided since they

were previously submitted to the United States Patent & Trademark Office in the above-identified parent application.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), within three (3) months of the filing date of the application.

RELEVANCE OF EACH DOCUMENT

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date 02/18/04

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: February 18, 2004

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Sheet 1 of 15

Complete if Known	
Application Number	Unassigned
Filing Date	February 18, 2004
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Group Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1	5,427,979		Chang	6/27/1995	
	A2	5,070,384		McCollum et al.	12/3/1991	
	A3	4,498,226		Inoue et al.	2/12/1985	
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	A6	5,745,407		Levy et al.	4/28/1998	
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	A36	5,675,547		Koga	10/7/1997	
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Examiner Signature		Date Considered	

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				Group Art Unit	Unassigned
(use as many sheets as necessary)				Examiner Name	Unassigned
Sheet	2	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS

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	A43	3,571,809		Nelson	3/23/1971	
	A44	3,573,757		Adams	4/6/1971	
	A45	3,699,543		Neale	10/17/1972	
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	A88	4,672,577		Hirose		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 3 of 15

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Group Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	035905-0134

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	A90	4,811,082		Jacobs		
	A91	5,001,539		Inoue et al.		
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Sheet	4	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS

		U.S. Patent Document				
	A135	6,314,013	B1	Ahn et al.		
	A136	6,322,903	B1	Siniaguine et al.		
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Examiner Initials*	Cite No.[1]	Foreign Patent Document: Office[3]	Number[4]	Kind Code[5] (*if known*)	Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	A141	EPO	0 073 486	A2	Toyama et al.	8-26-1982		Y
	A142	JP	61-222216		Takao	10-2-1986		Y
	A143	WO	94/26083		Carson et al.	11-10-1994		Y
	A144	EPO	0 516 866	A1	Bayer et al.	12-9-1992		Y
	A145	EPO	0 644 548	A2	Bertin	9-2-1994		Y
	A146	EPO	0 387 834	A2	Wada	9-14-1990		Y
	A147	EPO	0 800 137	A1	Genduso et al.	3-14-1997		Y
	A148	EPO	0 606 653	A1	Harward et al.	7-20-1994		Y
	A149	EPO	0 395 886	A2	Oota et al.	11-7-1990		Y
	A150	JP	63-52463		Hitachi Ltd	3-5-1998		Y
	A151	JP	6-22352		Fujitsu Ltd.	1-29-1994		Y
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	A153	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA	Y
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	A159	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE	Y
	A160	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs.301-305, VLSITSA	Y
	A161	VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE	Y
	A162	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE	Y
	A163	BOAZ EITAN et al.: "Multilevel Flash cells and their Trade-offs," IEEE Electron Device Letters , pgs. 169-172, 1996, IEEE	Y
	A164	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany	Y
	A165	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. sc-6, No. 5, October 1971	Y
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	A168	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE	Y

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	A169	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA	Y
	A170	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE	Y
	A171	J. ESQUIVEL et al. "High Density Contactless, Self Aligned EPROM Cell Array Technology," Texas Instruments (Dallas), IEDM 86, pgs. 592-595, 1986, IEEE	Y
	A172	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8μm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE	Y
	A173	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE	Y
	A174	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatle Memories," IEEE Transactions on Electron Devices , pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE	Y
	A175	WEB PAGE: JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation Web Page," VLSI Technology, 2000	Y
	A176	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE	Y
	A177	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE	Y

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	A178	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics	Y
	A179	K. MIYASHITA etal.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE	Y
	A180	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE	Y
	A181	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE	Y
	A182	WEB PAGE: M.C. POON. et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorpho Crystalline Silicon," IEEE Xplore Web Page, 1997	Y
	A183	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM 85, pgs. 639-642, 1985, IEEE	Y
	A184	TAKEO SHIBA et al.: "In Situ Phosphorus-Doped Polysilicon Emitter Technology for Very High-Speed, Small Emitter Bipolar Transistors," IEEE Transactions on Electron Devices , pgs. 889-897, Vol. 43, No. 6, June 1996, IEEE	Y
	A185	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE	Y
	A186	YOSHIHIRO TAKAO et al." "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE	Y

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	A188	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE	Y
	A189	HONGMEI WANG et al.: "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," IEEE Transactions on Electron Devices, pgs. 1580-1586, Vol. 47, No. 8, August 2000, IEEE	Y
	A190	MARVIN H. WHITE et al." "On the Go With Sonos," Circuit & Devices, pgs. 22-31, July 2000, IEEE	Y
	A191	B.J. WOO et al.: "A Novel Memory Cell Using Flash Array Contactless Eprom (Face) Technology," IEDM, pgs. 90-93, 1990, IEEE	Y
	A192	WEB PAGE: QI XIANG et al.: "Deep sub-100 nm CMOS with Ultra Low Gate Sheet Resista NiSi," IEEE Xplore Web Page, 2000	Y
	A193	QI XIANG et al."Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," IEEE, pgs. 76-77, 2000, Symposium on VLSI Technology Digest of Technical Papers	Y
	A194	QIUXIA XU et al.: "New Ti-SALICIDE Process Using Sb and Ge Preamorphization for Sub-0.2 μm CMOS Technology," IEEE Transactions on Electron Devices, pgs. 2002-2009, Vol. 45, No. 9, September 1998, IEEE	Y
	A195	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE	Y
	A196	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University, 1998	Y

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	A197	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE	Y
	A198	BRIAN DIPERT: "Exotic Memories, Diverse Approaches: Newfangled Memory Technologies Come and Go, But Every Once in a While, One Makes It Out of the Laboratory and Into Your Next Design. All of These Candidates Aspire to be the Next Semiconductor Success Story. Which Ones' Dreams Will Come True?" EDN ASIA web page (September 2001)	Y
	A199	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.	Y
	A200	YAMAZAKI K.: "4-Layer 3-D IC Technologies for Parallel Signal Processing", International Electron Devices Meeting Technical Digest, December 9-12, 1990, pgs 25.5.1 - 25.5.4.	Y
	A201	AKASAKA YOICHI: Three-dimensional Integrated Circuit: Technology and Application Prospect", Microelectronics Journal, Vol. 20, No.s 1-2, 1989, pgs. 105 - 112.	Y
	A202	SAKAMOTO KAJI: "Architecture des Circuits a Trois Dimension (Architecture of Three Dimensional Devices)", Bulletin of the Electrotechnical Laboratory, ISSN 0366-9092, Vol. 51, No. 1, 1987, pgs 16 - 29.	Y
	A203	AKASAKA YOICHI: "Three-dimensional IC Trends", "Proceedings of the IEEE, Vol. 74, No. 12, 1986, Pgs. 1703 - 1714.	Y
	A204	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuity".	Y
	A205	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	Y
	A206	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	Y
	A207	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	Y
	A208	BERTIN CLAUDE L.: "Evaluation of a Three-dimensional Memory Cube System", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, December 1993, pgs. 1006 - 1011.	Y

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	A209	WATANABE HIDEHIRO: "Stacked Capacitor Cells for High-density Dynamic RAMs", IEDM, 1988, pgs. 600 - 603.	Y
	A210	WEB PAGE: "Stacked Memory Modules", IBM Technical Disclosure Bulletin, Vol. 38, No. 5, 1995.	Y
	A211	THAKUR SHASHIDHAR: "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three VHV Channel Routing", IEDM, 1995, pgs. 207 - 210.	Y
	A212	TERRIL ROB: "3D Packaging Technology Overview and Mass Memory Applications", IEDM, 1996, pgs. 347 - 355.	Y
	A213	INOUE Y.: "A Three-Dimensional Static RAM", IEEE Electron Device Letters, Vol. 7, No. 5, May 1986, pgs. 327 - 329.	Y
	A214	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.	Y
	A215	KUROKAWA TAKAKAZU: "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction", FGCS - Future, Generation, Computer, Systems", Vol. 4, No. 2, 1988, pgs. 145-155, Amsterdam, The Netherlands.	Y
	A216	MAKINIAK DAVID: "Vertical Integration of Silicon Allows Packaging of Extremely Dense System Memory In Tiny Volumes: Memory-chip Stacks Send Density Skyward", Electronic Design, No. 17, August 22, 1994, pgs. 69-75, Cleveland Ohio.	Y
	A217	SCHLAEPPI H.P.: "nd Core Memories using Multiple Coincidence", IRE Transactions on Electronic Computers, June 1960, pgs 192 - 196.	Y
	A218	SCHLAEPPPPI H.P.: "Session V: Information Storage Techniques", International Solid-State Circuits Conference, February 11, 1960, pgs. 54-55.	Y
	A219	YAMAZAKI K.: "Fabrication Technologies for Dual 4-KBIT Stacked SRAM", IEDM 16.8., 1986, pgs. 435-438.	Y
	A220	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189	Y

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	A221	PETER K. NAJI et al.: "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM," 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001, pp. 122-123 (including enlargement of figures, totaling 9 pages), and associated Visual Supplement, pp. 94-95,4040-405 (enlargements of slides submitted, totaling 25 pages)	Y
	A222	KIM C. HARDEE et al.: "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM," IEEE Journal of Solid-State Circuits, October 1981, Vol. SC-16, No. 5, pages 435-443	Y
	A223	TOSHIO WADA et al.: "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, October 1978, Vol. SC-13, No. 5, pages 635-639	Y
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	A225	PEIN HOWARD: "Performance of the 3-D PENCIL Flash EPROM Cell an Memory Array", IEEE Transactions on Electron Devices, Vol. 42, No. 11, November 1995, pgs. 1982-1991.	Y
	A226	Abstract LOMATCH S.: "Multilayered Josephson Junction Logic and Memory Devices", Proceedings of the SPIE-The International Society for Optical Engineering Vol. 2157, pgs. 332-343.	Y
	A227	Abstract LU N.C.C.: "Advanced Cell Structures for Dynamic RAMs", IEEE Circuits and Devices Magazine, Vol. 5, No. 1, January 1989, pgs. 27-36.	Y
	A228	Abstract SAKAMATO K.: "Architecture of Three Dimensional Devices", Journal: Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pgs. 16-29.	Y
	A229	Abstract "Wide Application of Low-Cost Associative Processing Associative Processing Seen", Electronic Engineering Times, August 26, 1996, pg. 43.	Y
	A230	Abstract "Interconnects & Packaging", Electronic Engineering Times, November 27, 1995, pg. 43.	Y
	A231	Abstract "Closing in on Gigabit DRAMs", Electronic Engineering Times, November 27, 1995, pg. 35.	Y
	A232	Abstract "Module Pact Pairs Cubic Memory with VisionTek", Semiconductor Industry & Business Survey, Vol. 17, No. 15, October 23, 1995.	Y

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	A233	Abstract "Layers of BST Materials Push Toward 1Gbit DRAM", Electronics Times, October 19, 1995.	Y
	A234	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.	Y
	A235	Abstract "Looking Diverse Storage", Electronic Engineering Times, October 31, 1994, pg. 44.	Y
	A236	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.	Y
	A237	Abstract "Technique Boosts 3D Memory Density", Electronic Engineering Times, August 29, 1994, pg. 16.	Y
	A238	Abstract "Memory Packs Poised 3D Use", Electronic Engineering Times, December 7, 1992, pg. 82.	Y
	A239	Abstract "MCMs Hit the Road", Electronic Engineering Times, June 15, 1992, pg. 45.	Y
	A240	Abstract "IEDM Ponders the 'Gigachip' Era", Electronic Engineering Times, January 20, 1992, pg. 33.	Y
	A241	Abstract "Tech Watch: 1-Gbit DRAM in Sight", Electronic World News, December 16, 1991, pg. 20.	Y
	A242	Abstract "MCMs Meld into Systems", Electronic Engineering Times, July 22, 1991, pg. 35.	Y
	A243	Abstract "Systems EEs See Future in 3D", Electronic Engineering Times, September 24, 1990, pg. 37.	Y
	A244	Patent Application, NISHIURA, US 2001/00054759 A1.	Y

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	Unassigned
				Filing Date	February 18, 2004
Date Submitted: February 18, 2004				**First Named Inventor**	Kedar PATEL et al.
				Group Art Unit	Unassigned
(use as many sheets as necessary)				Examiner Name	Unassigned
Sheet	13	of	15	Attorney Docket Number	035905-0134

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	A245	Patent Application, FURUSAWA, US 2002/0024146 A1.	Y
	A246	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.	Y
	A247	Patent Application, AKRAM, US 2002/0030262 A1.	Y
	A248	Patent Application, AKRAM, US 2002/0030263 A1.	Y
	A249	Patent Application, LEEDY, US 2001/0033030 A1.	Y

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Sheet	14	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A250	6,110,278		Saxena	8/29/2000	
	A251	RE37,259	E	Ovshinsky	7/3/2001	
	A252	2001/0055838	A1	Walker, et al	12/27/2001	
	A253	2002/0028541	A1	Lee, et al.	3/7/2002	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	A254	"3D Chip-On-Chip Stacking," Semiconductor International, December 1991	Y
	A255	RICHARD W. LAY: "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1994	Y

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	A256	5,517,038		Maeda et al.	5/14/1996	
	A257	5,770,483		Kadosh et al.	6/23/1998	
	A258	6,593,624		Walker	7/15/2003	
	A259	2003/0030074	A1	Walker et al.	2/13/2003	
	A260	2003/0173643		Herner	9/18/2003	
	A261	2002/0142546	A1	Kouznetsov	10/3/2002	
	A262	2003/0057435	A1	Walker	3/27/2003	

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